

Title:	PROGRAMMING NON-VOLATILE MEMORY	Docket No.:	SAND-01017US0
Applicants:	Hemink, et al.	Atty:	Burt Magen
Appl. No.:	Unknown	Phone:	(415) 369-9660
Filing Date:	January 21, 2004		
Express Mail No.:	EL 994 763 485 US		

Fig. 1

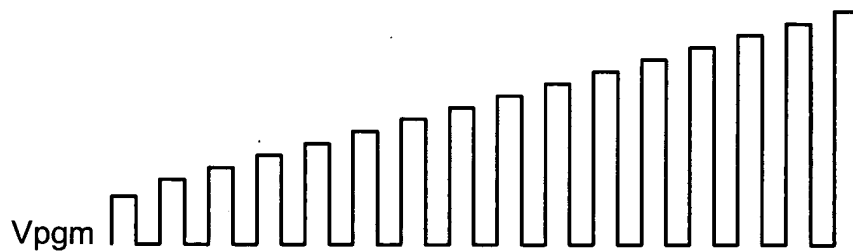
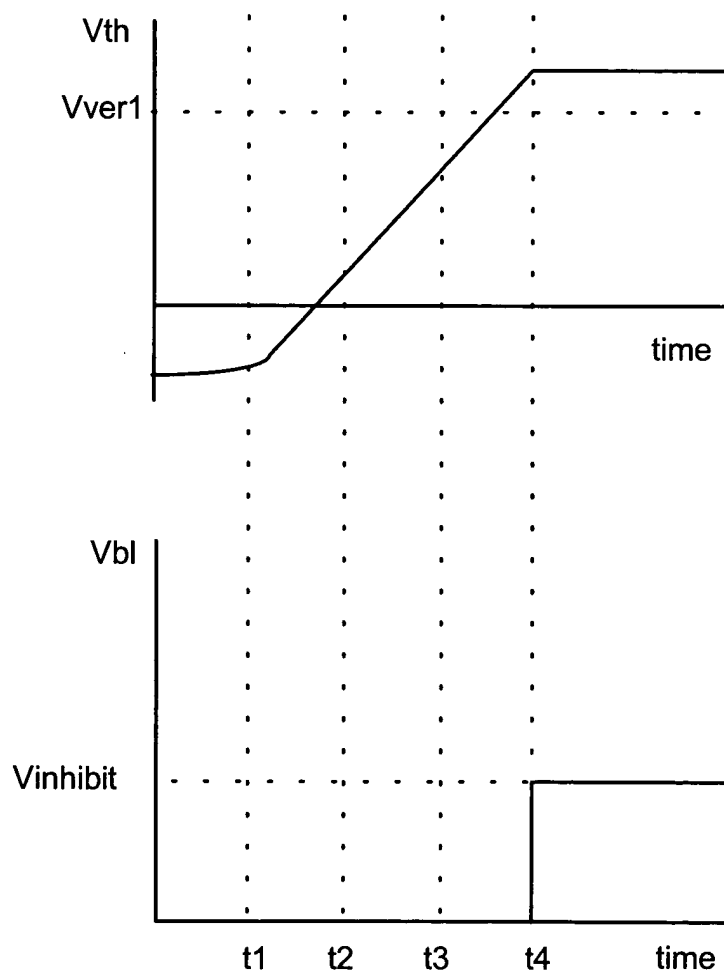
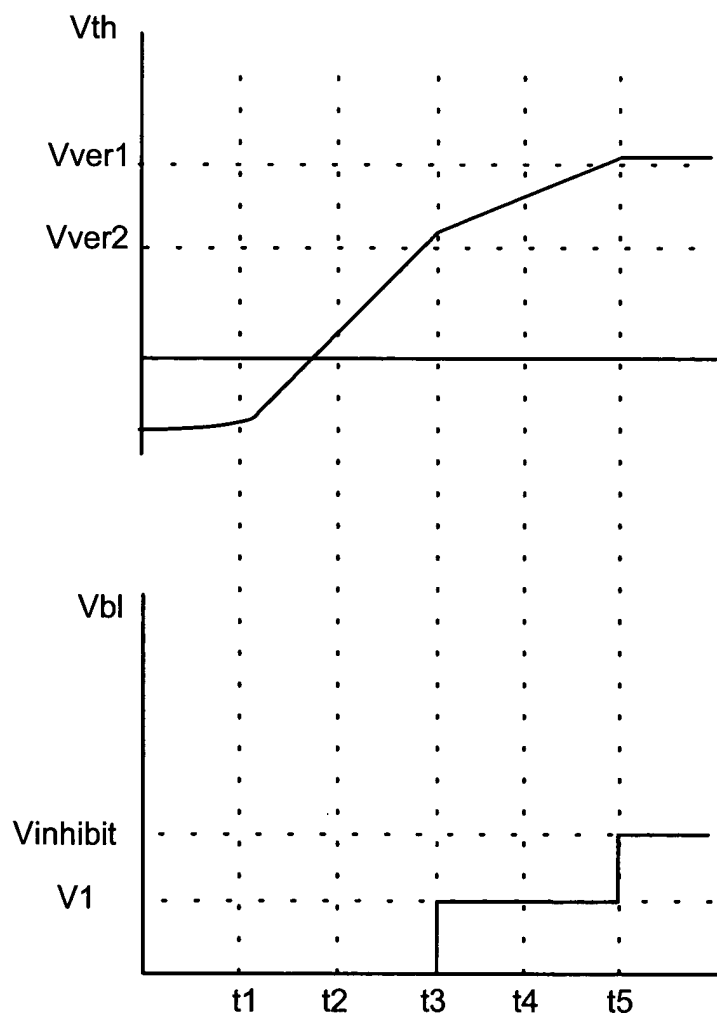


Fig. 2 (Prior Art)



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Fig. 3 (Prior Art)



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Fig. 4

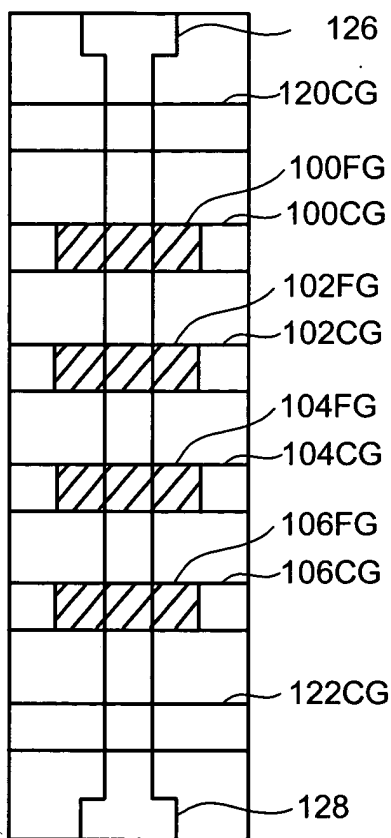


Fig. 5

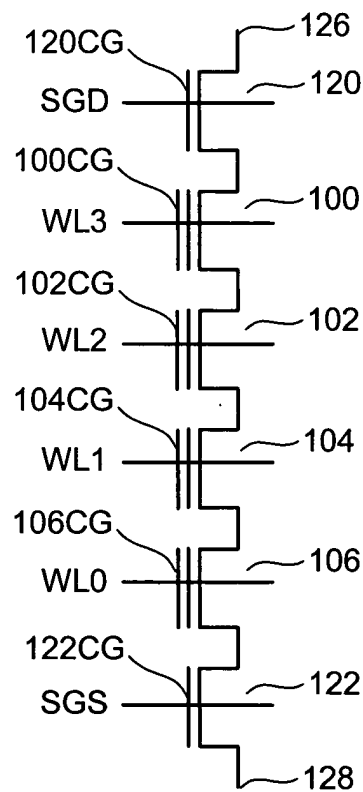
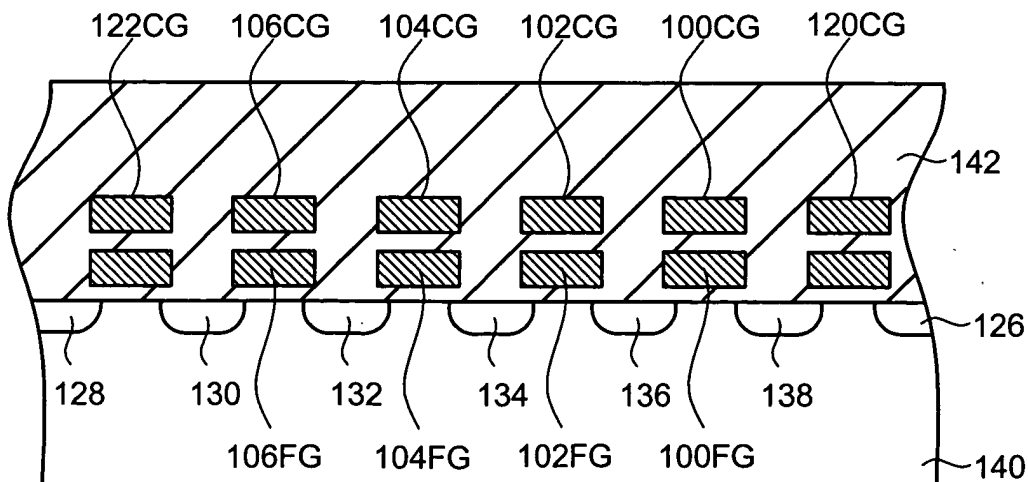


Fig. 6

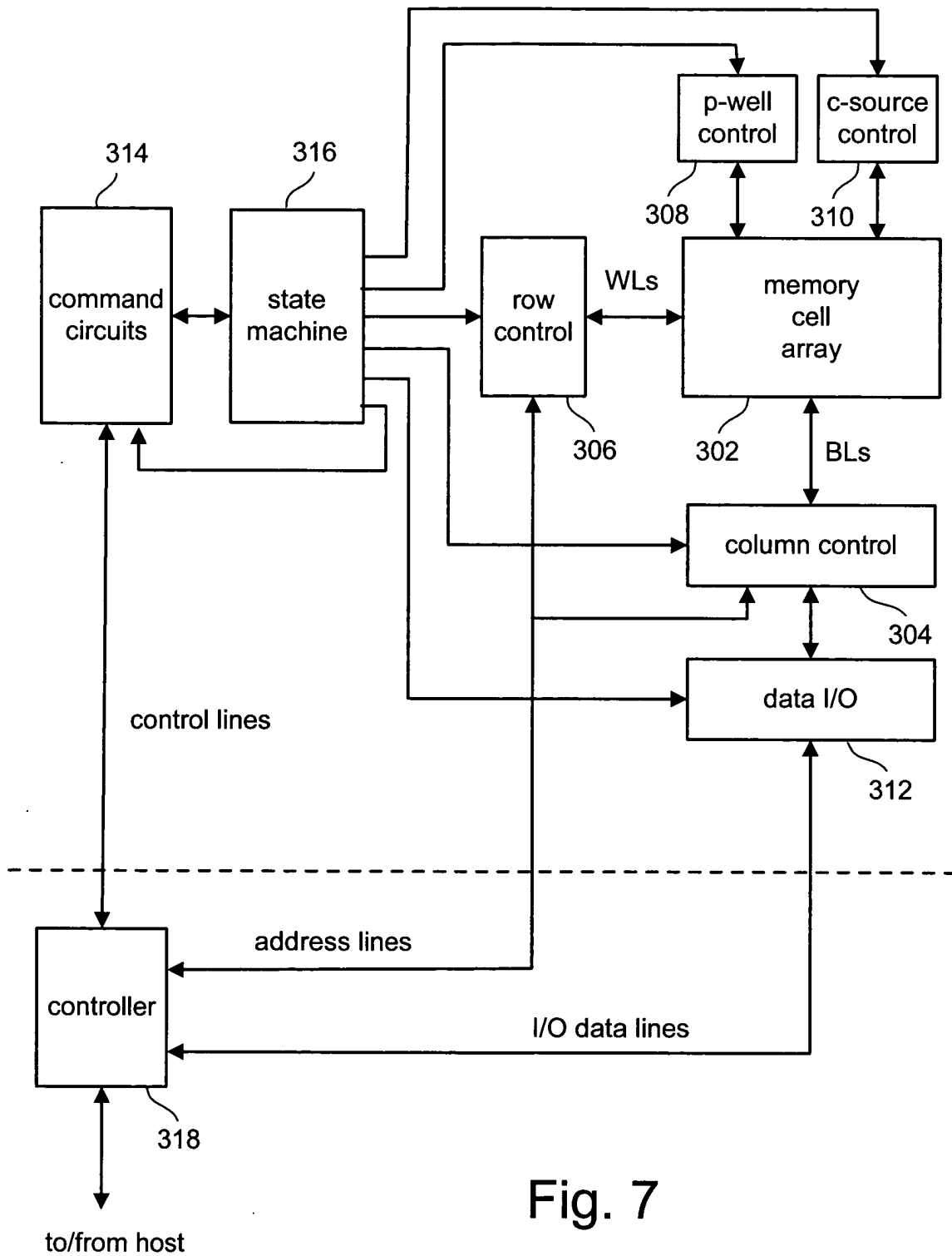


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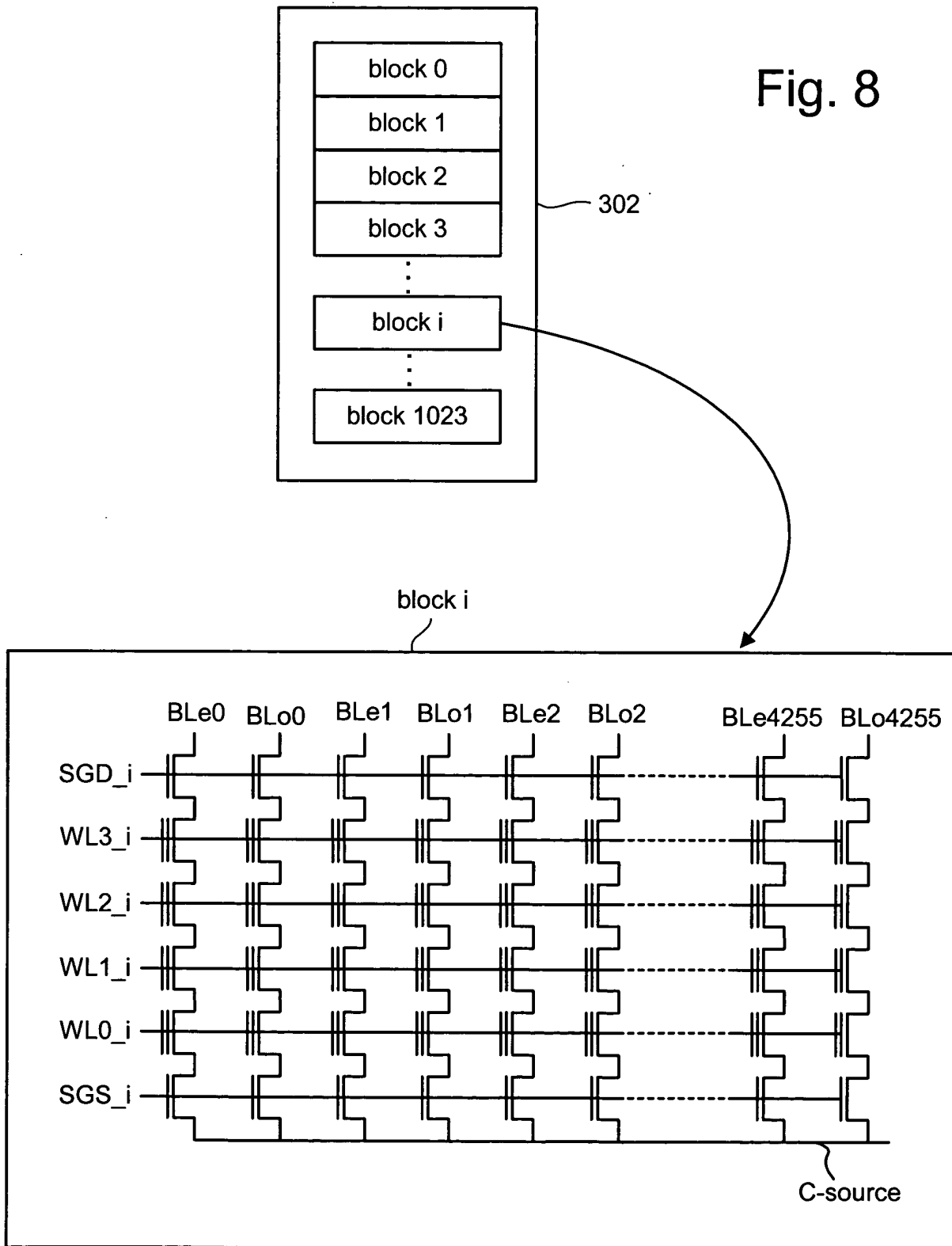


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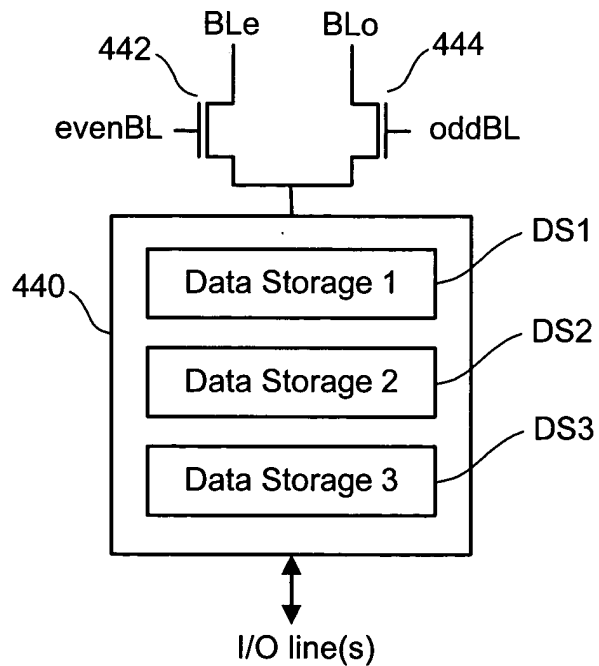


Fig. 9

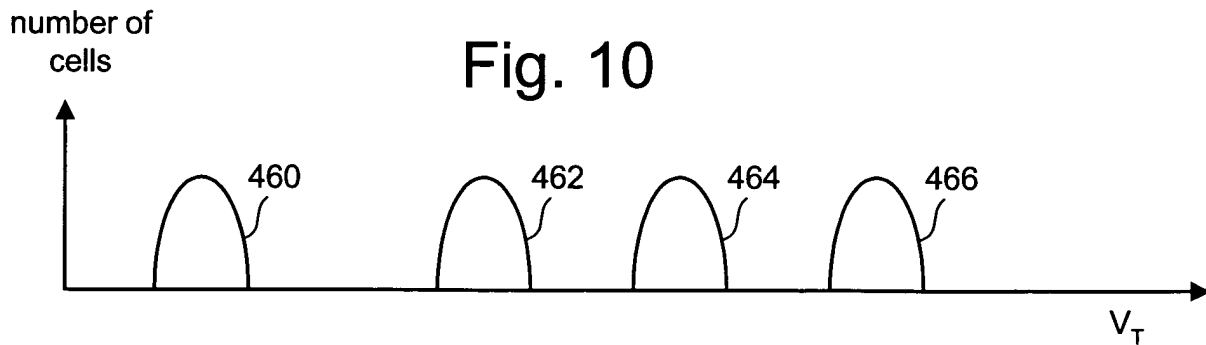
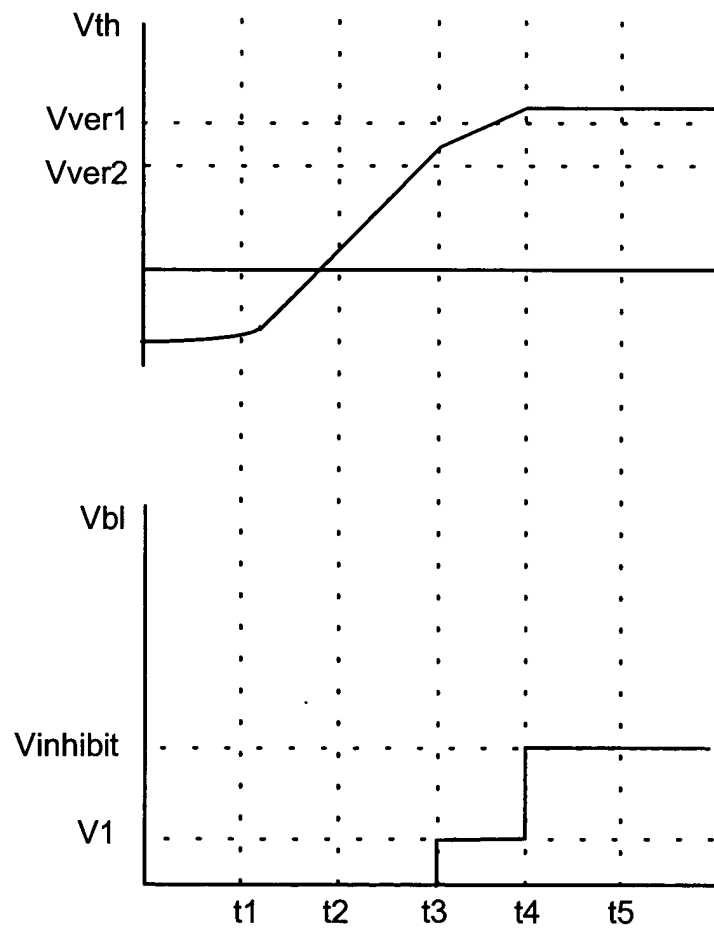


Fig. 10

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Fig. 11



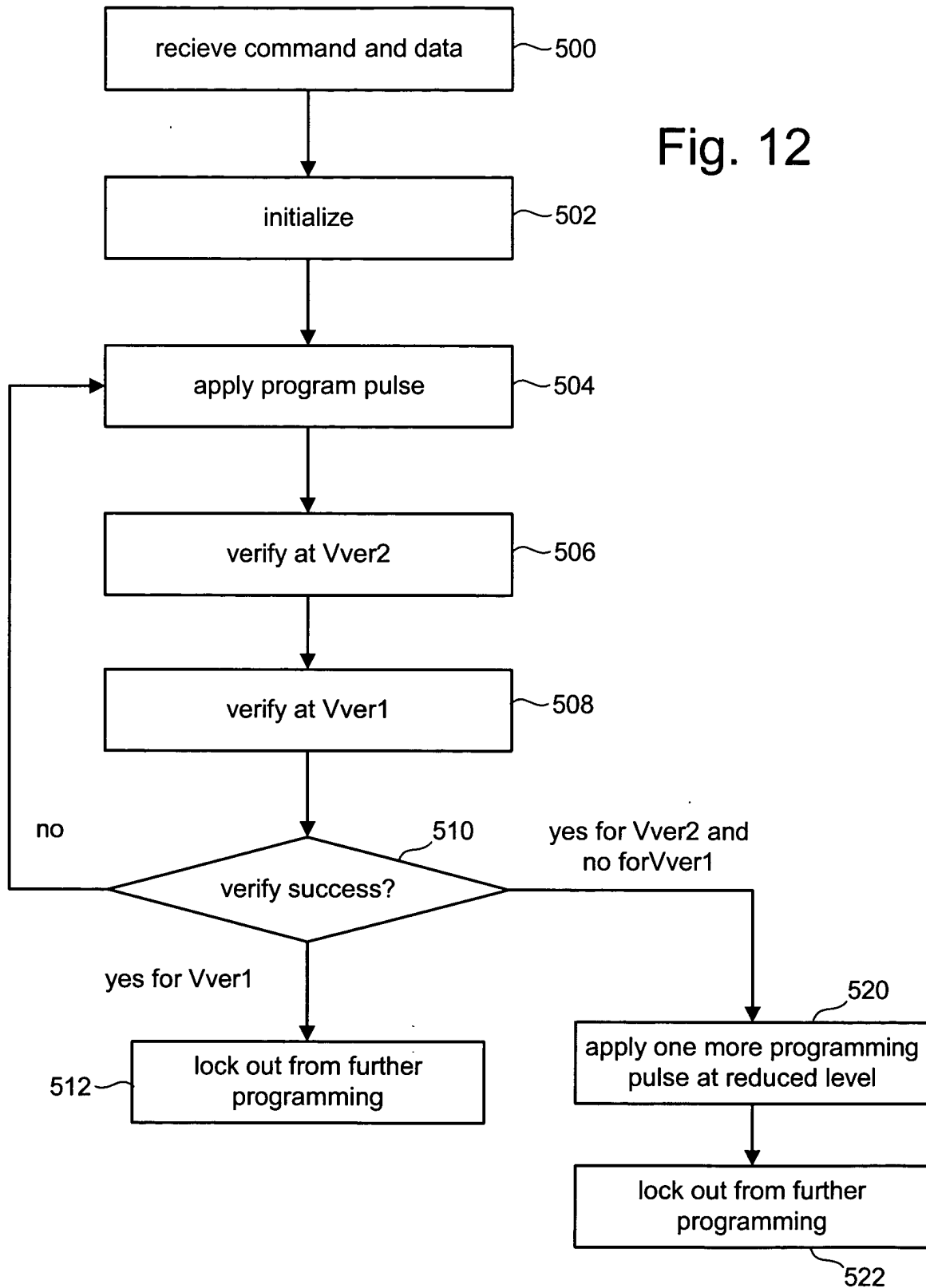
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Fig. 12



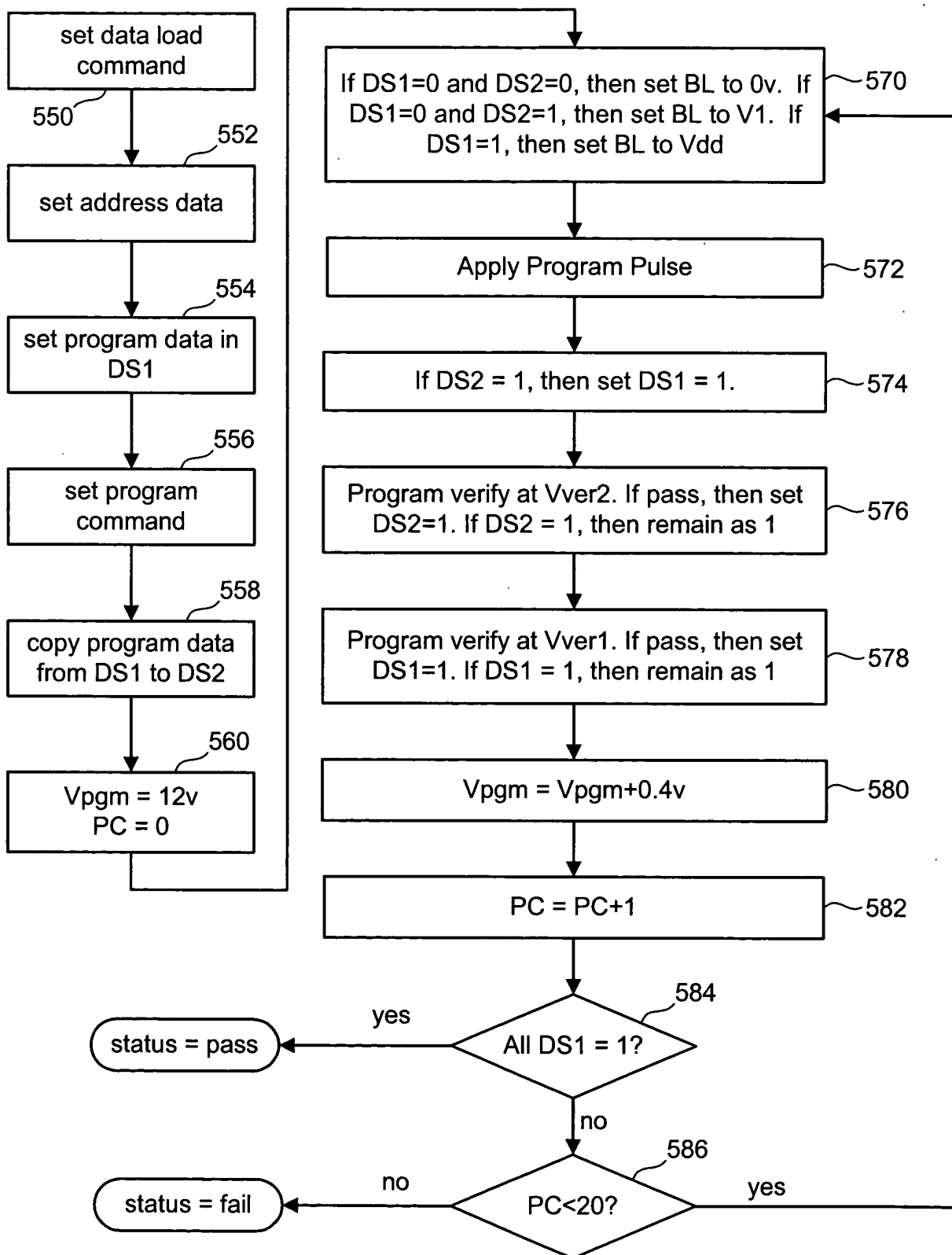


Fig. 13

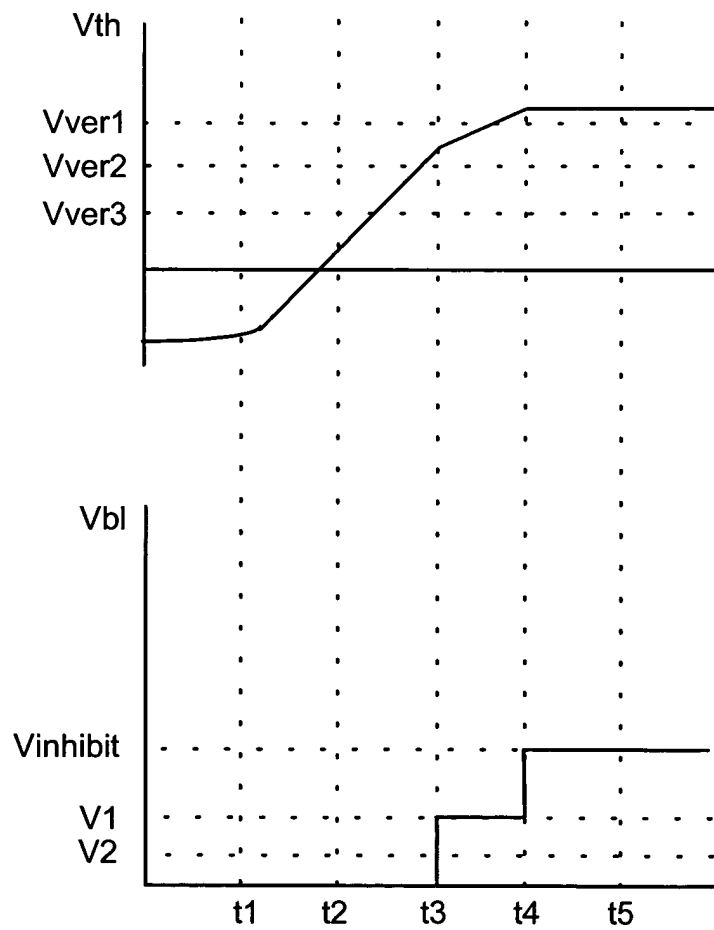
Fig. 14

```
graph TD
    620[set data load command] --> 622[set address data]
    622 --> 624[set program data in DS1]
    624 --> 626[set program command]
    626 --> 628[copy program data from DS1 to DS2]
    628 --> 630["10- read  
If pass, then DS3=1,  
else DS3=0"]
    630 --> 632["Vpgm = 13v  
PC = 0"]
    632 --> 640["If DS1=0 and DS2=0, then set BL  
to 0v. If DS1=0 and DS2=1, then  
set BL to V1. If DS1=1, then set  
BL to Vdd"]
    640 --> 642[Apply Program Step]
    642 --> 644["If DS2 = 1, then set DS1 = 1."]
    644 --> 646["00 - Program verify at Vver2. If  
DS3=1 and pass, then set DS2=1.  
If DS2 = 1, then remain as 1"]
    646 --> 648["00 - Program verify at Vver1. If  
DS3=1 and pass, then set DS1=1."]
    648 --> 650["01 - Program verify at Vver2. If  
DS3=0 and pass, then set DS2=1.  
If DS2 = 1, then remain as 1"]
    650 --> 652["01 - Program verify at Vver1. If  
DS3=0 and pass, then set DS1=1."]
    652 --> 654["Vpgm = Vpgm+0.4v"]
    654 --> 656["PC = PC+1"]
    656 --> 658{"All DS1 = 1?"}
    658 -- yes --> 640
    658 -- no --> 660{"PC < 20?"}
    660 -- yes --> 640
    660 -- no --> fail(status = fail)
    fail --> 640
```

The flowchart illustrates a programming sequence for a memory device. It begins with a series of initialization steps: setting a data load command (620), address data (622), program data in DS1 (624), program command (626), and copying program data from DS1 to DS2 (628). A read operation (630) is performed, where DS3 is set to 1 if the pass and 0 otherwise. The programming voltage (Vpgm) is set to 13v and the program counter (PC) is set to 0 (632). The main programming loop starts with setting the bit line (BL) based on DS1 and DS2 values (640). An "Apply Program Step" (642) is then executed. Subsequent steps (644, 646, 648, 650, 652) involve program verification at different voltages (Vver1, Vver2) and setting DS1 or DS2 to 1 based on the verification results. The programming voltage (Vpgm) is incremented by 0.4v (654), and the program counter (PC) is incremented by 1 (656). A decision is made on whether all DS1 values are 1 (658). If yes, the loop returns to step 640. If no, a decision is made on whether PC is less than 20 (660). If yes, the loop returns to step 640. If no, the status is set to "fail" (660), which then loops back to step 640.

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Fig. 15



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Fig. 16

